What Is Claimed Is:

1. A circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor; and

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor.

2. The system of claim 1 wherein an operating system executes on the processor.

3. The system of claim 1 wherein the hang detector module detects the hang in the co-processor by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor.

4. The system of claim 3 wherein the discrepancy is detected by detecting the current state to be busy, by detecting a busy flag to be set, and detecting no progress on current activity, by detecting the same contents in a co-processor register as examined before and after a wait period.

5. The system of claim 1 further comprising:

a halt communications module operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor;

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor; and

a restart communications module operative to restart command communications with the co-processor, in response to detecting that the co-processor has been successfully reset.

6. A method of monitoring and resetting a co-processor comprising the steps of:

detecting a hang in the co-processor; and

selectively resetting the co-processor without resetting a processor, in response to detecting a hang in the co-processor.

7. The method of claim 6 wherein an operating system executes on the processor.

8. The method of claim 6 wherein detecting a hang in the co-processor is performed by detecting a discrepancy between a current state of the co-processor and a current activity of the co-processor.

9. The method of claim 8 wherein the wherein the discrepancy is detected by detecting the current state to be busy, by detecting a busy flag to be set, and detecting no progress on current activity, by detecting the same contents in a co-processor register as examined before and after a wait period.

10. The method of claim 6 further comprising the step of:

halting command communications with the co-processor, in response to detecting a hang in the co-processor;

detecting if the co-processor has been successfully reset, in response to the resetting of the co-processor; and

restarting command communications with the co-processor, in response to detecting that the co-processor has been successfully reset.

11. A circuit for monitoring and resetting a co-processor comprising:

a hang detector module operative to detect a hang in the co-processor;

a halt communications module operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor;

a selective processor reset module operative to selectively reset the co-processor without resetting a processor, in response to detecting a hang in the co-processor;

a reset check module operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor; and

a restart communications module operative to restart command communications with the co-processor, in response to detecting that the co-processor has been successfully reset.

12. The circuit of claim 11 wherein the processor is a host processor and the co-processor is a graphics processor.

13. The circuit of claim 12 wherein the hang detector module detects the hang in the graphics processor by detecting a discrepancy between a current state of the graphics processor and a current activity of the graphics processor.

14. A system for monitoring and resetting a co-processor comprising:

a processor;

a co-processor; and

a memory containing instructions including:

hang detector module instructions operative to detect a hang in the co-processor; and

selective processor reset module instructions operative to selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor.

15. The circuit of claim 14 wherein the processor is a host processor and the memory contains operating system instructions.

16. The system of claim 14 wherein the hang detector module instructions detect the hang in the co-processor by detecting the current state to be busy, as reflected in a busy flag, and detecting no progress on current activity, as reflected the absence of co-processor register activity.

17. The system of claim 14 further comprising:

reset check module instructions operative to detect if the co-processor has been successfully reset, in response to the resetting of the co-processor.

18. The system of claim 14 further comprising:

halt communications module instructions operative to halt command communications with the co-processor, in response to detecting a hang in the co-processor; and

restart communications module instructions operative to restart command communications with the co-processor, in response to detecting that the co-processor has been successfully reset.

19. A system for monitoring and resetting a co-processor comprising:

a host processor;

a graphics processor; and

a memory containing instructions including:

hang detector module instructions operative to detect a hang in the graphics processor; and

selective processor reset module instructions operative to selectively reset the graphics processor without resetting the host processor, in response to detecting a hang in the graphics processor.

20. The system of claim 19 wherein the hang detector module instructions detect the hang in the graphics processor by detecting the current state of the graphics processor to be busy, as reflected in a graphics processor busy flag, and detecting the current activity of the graphics processor to be idle, as reflected in the absence of graphics processor register activity.

21. The system of claim 19 further comprising:

halt communications module instructions operative to halt rendering command communications with the graphics processor, in response to detecting a hang in the graphics processor;

reset check module instructions operative to detect if the graphics processor has been successfully reset, in response to the resetting of the graphics processor; and

restart communications module instructions operative to restart rendering command communications with the graphics processor, in response to detecting that the graphics processor has been successfully reset.

22. A system for monitoring and resetting a co-processor comprising:

a host processor;

a graphics processor; and

a memory containing instructions including:

hang detector module instructions operative to detect a hang in the graphics processor by detecting the current state to be busy, by detecting a busy flag to be set, and detecting no progress on current activity, by detecting the same contents in a co-processor register as examined before and after a wait period;

halt communications module instructions operative to halt rendering command communications with the graphics processor by setting a send flag to an off state and setting a receive flag to an off state, in response to detecting a hang in the graphics processor;

save snapshot module instructions operative to save a snapshot of the hardware and software status including any one or more of the following: graphics register data, graphics command queue data, chipset info, and AGP bus status, in response to the detecting a hang in the graphics processor;

selective processor reset module instructions operative to selectively reset the graphics processor without resetting the host processor, in response to detecting a hang in the graphics processor;

reset check module instructions operative to detect if the graphics processor has been successfully reset, in response to the resetting of the graphics processor;

display mode switch module instructions operative to perform a display mode switch, in response to the selectively resetting of the graphics processor;

functioning check module instructions operative to detect if the graphics processor is fully functioning, in response to the resetting of the graphics processor;

restart communications module instructions operative to restart rendering command communications with the graphics processor by setting the send flag to an on state, in response to detecting that the graphics processor has been successfully reset; and

software rendering module instructions operative to dynamically switch to software rendering mode, in response to detecting any one or more of the following: a detection that the graphics processor has not been successfully reset and a detection that the graphics processor is not fully functioning.

23. The system of claim 22 further comprising:

hang resolved prompt module instructions operative to display a prompt indicating that a hang was detected and resolved, in response to detecting that the graphics processor is fully functioning;

report send prompt module instructions operative to display a prompt requesting an input as to whether a user wants to have an error report sent to a remote location, in response to detecting a hang in the graphics processor;

report send module instructions operative to send an error report to a remote location including the hardware and software status, in response to receiving a user request to send an error report to a remote location; and

hang unresolved prompt module instructions operative to display a prompt indicating that a hang was detected and cannot be resolved without a reset of the host processor being performed, in response to detecting one or more of the following: the graphics processor was not successfully reset and the graphics processor is not fully functioning.

24. A memory containing instructions executable on a processor that causes the processor to:

detect a hang in a co-processor; and

selectively reset the co-processor without resetting the processor, in response to detecting a hang in the co-processor.

25. The memory of claim 24 further including instructions that causes the processor to:

detect if the co-processor has been successfully reset, in response to the resetting of the co-processor.